

# DATA SHEET

## **TDA1543**

**Dual 16-bit DAC (economy version)  
(I<sup>2</sup>S input format)**

Product specification  
File under Integrated Circuits, IC01

February 1991

## Dual 16-bit DAC (economy version) (I<sup>2</sup>S input format)

TDA1543

### FEATURES

- Low distortion
- 16-bit dynamic range
- 4 × oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- I<sup>2</sup>S input format: time multiplexed, two's complement, TTL.

### GENERAL DESCRIPTION

The TDA1543 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders, digital sound in TV sets and in digital amplifiers.

### ORDERING INFORMATION

| EXTENDED<br>TYPE NUMBER | PACKAGE |              |          |               |
|-------------------------|---------|--------------|----------|---------------|
|                         | PINS    | PIN POSITION | MATERIAL | CODE          |
| TDA1543 <sup>(1)</sup>  | 8       | DIL          | plastic  | SOT97         |
| TDA1543T <sup>(2)</sup> | 16      | mini-pack    | plastic  | SO16L;SOT162A |

### Notes

1. SOT97-1; 1996 August 13.
2. SOT162-1 1996 August 13.

### QUICK REFERENCE DATA

| SYMBOL            | PARAMETER                              | CONDITIONS                      | MIN. | TYP.                     | MAX.  | UNIT            |
|-------------------|--|---------------------------------|------|--------------------------|-------|-----------------|
| V <sub>DD</sub>   | supply voltage                         |                                 | 3.0  | 5.0                      | 8.0   | V               |
| I <sub>DD</sub>   | supply current                         |                                 | –    | 50                       | 60    | mA              |
| I <sub>FS</sub>   | full scale output current              |                                 | 1.95 | 2.30                     | 2.65  | mA              |
| THD               | total harmonic distortion              | including noise<br>at 0 dB      | –    | –75                      | –70   | dB              |
|                   |  |                                 | –    | 0.018                    | 0.032 | %               |
| THD               | total harmonic distortion              | including noise<br>at –60 dB    | –    | –30                      | –23   | dB              |
|                   |  |                                 | –    | 3.2                      | 7.9   | %               |
| t <sub>CS</sub>   | current settling time to ± 1 LSB       |                                 | –    | 0.5                      | –     | µs              |
| BR                | input bit rate at data input           |                                 | –    | –                        | 9.2   | Mbits/s         |
| f <sub>BCK</sub>  | clock frequency at clock input         |                                 | –    | –                        | 9.2   | MHz             |
| S/N               | signal-to-noise ratio                  | at bipolar zero                 | 90   | 96                       | –     | dB              |
| TC <sub>FS</sub>  | full scale temperature coefficient     | at analog outputs<br>(AOL; AOR) | –    | ± 500 × 10 <sup>–6</sup> | –     | K <sup>–1</sup> |
| T <sub>amb</sub>  | operating ambient temperature<br>range |                                 | –30  | –                        | +85   | °C              |
| P <sub>tot</sub>  | total power dissipation                |                                 | –    | 250                      | –     | mW              |
| I <sub>bias</sub> | bias current (adjustable)              |                                 | –0.6 | –                        | 5.0   | mA              |

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(I<sup>2</sup>S input format)

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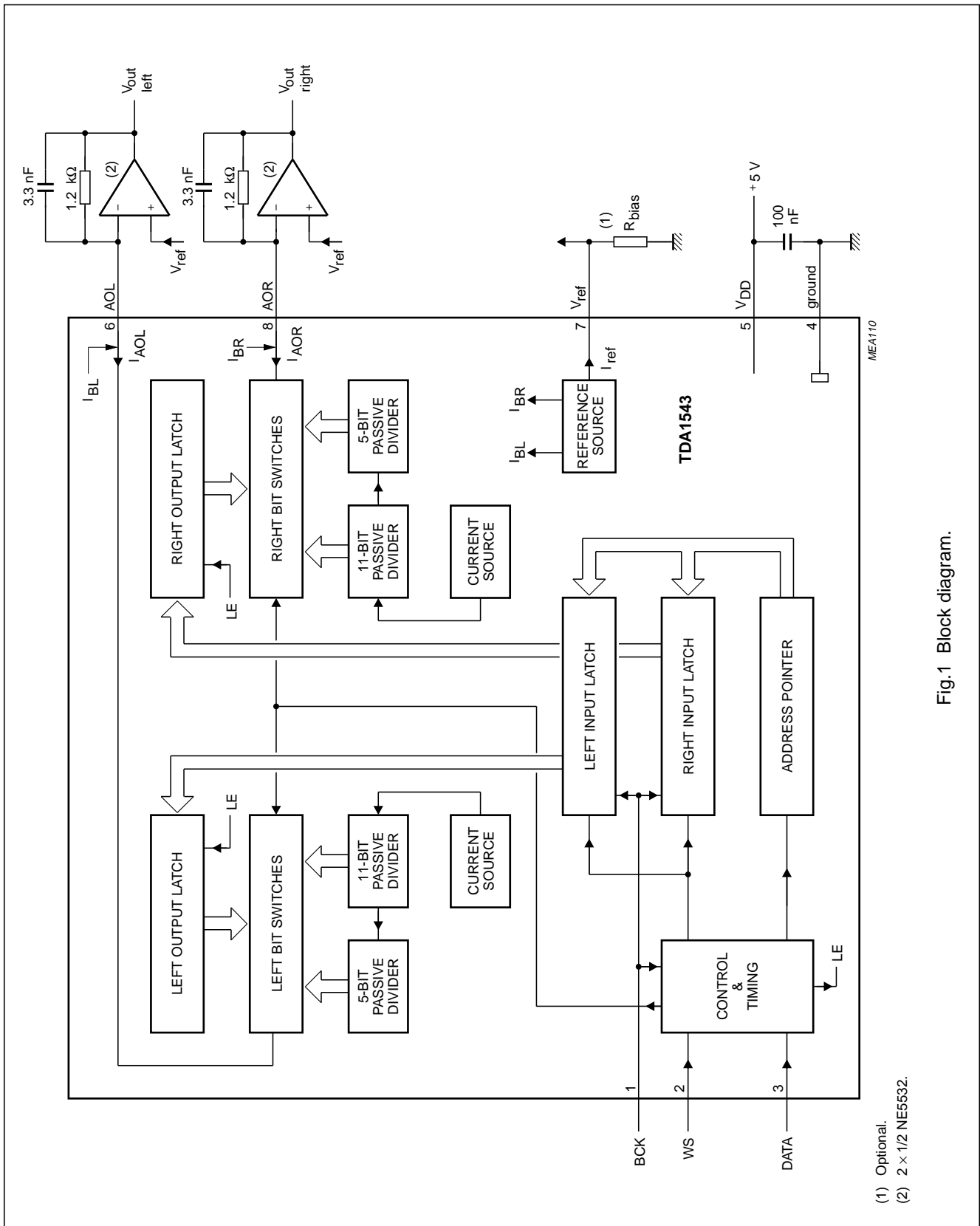


Fig.1 Block diagram.

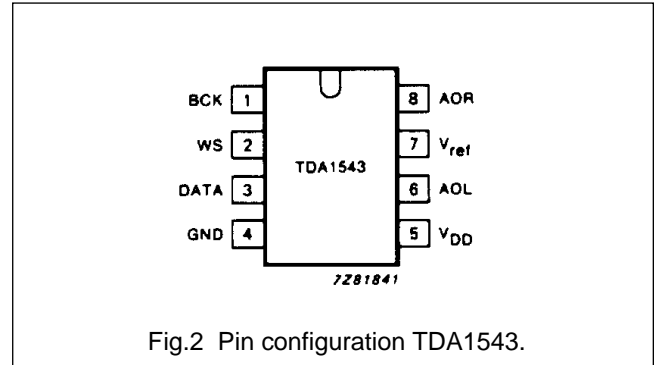
(1) Optional.  
(2) 2 × 1/2 NE5532.

Dual 16-bit DAC (economy version)  
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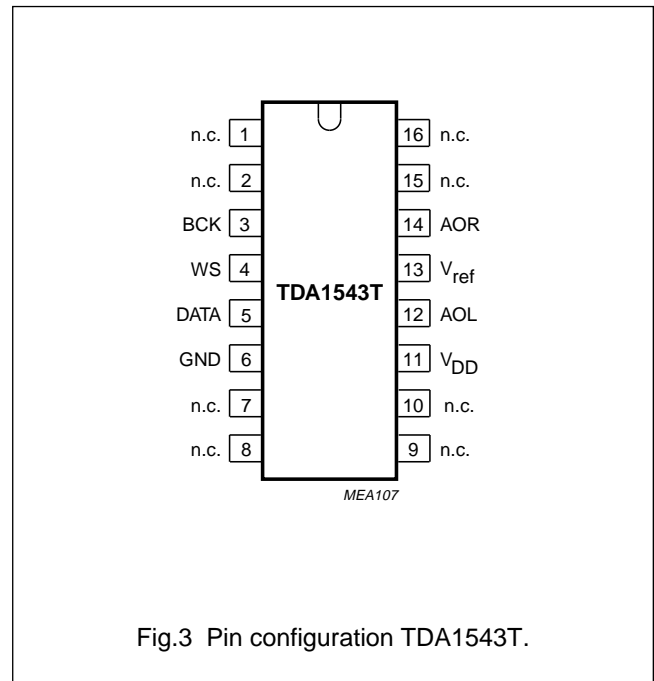
**PINNING**

| SYMBOL           | PIN | DESCRIPTION                 |
|------------------|-----|-----------------------------|
| BCK              | 1   | bit clock input             |
| WS               | 2   | word select input           |
| DATA             | 3   | data input                  |
| GND              | 4   | ground                      |
| V <sub>DD</sub>  | 5   | +5 V supply voltage         |
| AOL              | 6   | left channel voltage output |
| V <sub>ref</sub> | 7   | reference voltage output    |
| AOR              | 8   | right channel output        |



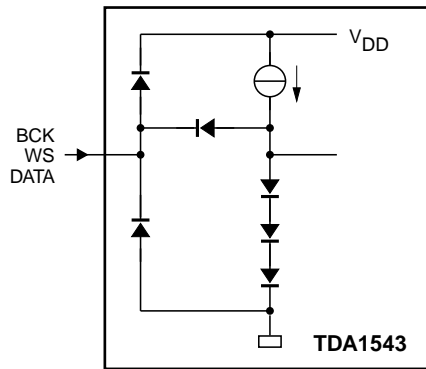
**PINNING**

| SYMBOL           | PIN | DESCRIPTION              |
|------------------|-----|--------------------------|
| n.c.             | 1   | not connected            |
| n.c.             | 2   | not connected            |
| BCK              | 3   | bit clock input          |
| WS               | 4   | word select input        |
| DATA             | 5   | data input               |
| GND              | 6   | ground                   |
| n.c.             | 7   | not connected            |
| n.c.             | 8   | not connected            |
| n.c.             | 9   | not connected            |
| n.c.             | 10  | not connected            |
| V <sub>DD</sub>  | 11  | +5 V supply voltage      |
| AOL              | 12  | left channel output      |
| V <sub>ref</sub> | 13  | reference voltage output |
| AOR              | 14  | right channel output     |
| n.c.             | 15  | not connected            |
| n.c.             | 16  | not connected            |

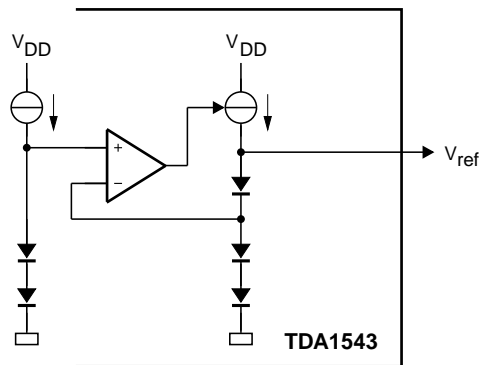


Dual 16-bit DAC (economy version)  
(I<sup>2</sup>S input format)

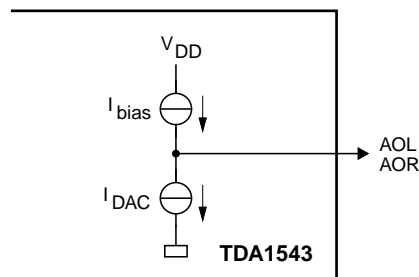
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(a) input pins BCK, WS and DATA.



(b) output pin V<sub>ref</sub>.



(c) output pins AOL and AOR.

MEA109

Fig.4 Circuits at the input and output pins.

## Dual 16-bit DAC (economy version) (I<sup>2</sup>S input format)

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### FUNCTIONAL DESCRIPTION

The TDA1543 accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.5 and Fig.6.

This flexible input data format (I<sup>2</sup>S) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processor circuits (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 × oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the left input register and with a HIGH level on the WS input data is placed in the right input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current  $I_{ref}$  at the  $V_{ref}$  output is adjusted by a resistor or a current source. The current  $I_{ref}$  is amplified with gain  $A_{bias}$  to the bias currents ( $I_{BL}$ ;  $I_{BR}$ ) which are added to the output currents.

### LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

| SYMBOL     | PARAMETER                           | CONDITIONS | MIN.  | MAX.  | UNIT |
|------------|-------------------------------------|------------|-------|-------|------|
| $V_{DD}$   | supply voltage range                |            | 0     | 9     | V    |
| $T_{XTAL}$ | crystal temperature                 |            | –     | +150  | °C   |
| $T_{stg}$  | storage temperature range           |            | –55   | +150  | °C   |
| $T_{amb}$  | operating ambient temperature range |            | –30   | +85   | °C   |
| $V_{es}$   | electrostatic handling*             |            | –2000 | +2000 | V    |

### THERMAL RESISTANCE

| SYMBOL        | PARAMETER                | TYP. | UNIT |
|---------------|--------------------------|------|------|
| $R_{th\ j-a}$ | from junction to ambient | 100  | K/W  |

\* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

## Dual 16-bit DAC (economy version) (I<sup>2</sup>S input format)

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### CHARACTERISTICS

$V_{DD} = 5\text{ V}$ ;  $T_{amb} = +25\text{ °C}$ ;  $I_{ref} = 0\text{ mA}$ ; measured in the circuit of Fig.1; unless otherwise specified

| SYMBOL                                       | PARAMETER   | CONDITIONS                                     | MIN. | TYP.                     | MAX.           | UNIT            |
|--|---|--|------|--------------------------|----------------|-----------------|
| <b>Supply</b>                                |   |  |      |                          |                |                 |
| $V_{DD}$                                     | supply voltage range                                  |  | 3.0  | 5.0                      | 8.0            | V               |
| $I_{DD}$                                     | supply current  | note 1   | –    | 50                       | 60             | mA              |
| RR   | ripple rejection                                      | note 2   | –    | 50                       | –              | dB              |
| <b>Digital inputs</b>                        |   |  |      |                          |                |                 |
| $I_{IL}$                                     | input current pins (1, 2 and 3)<br>digital inputs LOW | $V_I = 0.8\text{ V}$                           | –    | –                        | –0.4           | mA              |
| $I_{IH}$                                     | digital inputs HIGH                                   | $V_I = 2.0\text{ V}$                           | –    | –                        | 20             | $\mu\text{A}$   |
| $f_{BCK}$                                    | input frequency/bit rate<br>clock input pin 1         |  | –    | –                        | 9.2            | MHz             |
| BR   | bit rate data input pin 3                             |  | –    | –                        | 9.2            | Mbits/s         |
| $f_{WS}$                                     | word select input pin 2                               |  | –    | –                        | 192            | kHz             |
| <b>Analog outputs (AOL; AOR)</b>             |   |  |      |                          |                |                 |
| Res  | resolution  |  | –    | –                        | 16             | bits            |
| $V_{OC(AC)}$                                 | output voltage compliance<br>AC                       |  | –    | $\pm 25$                 | –              | mV              |
| $V_{OC(DC)}$                                 | DC  |  | 1.8  | –                        | $V_{DD} - 1.2$ | V               |
| $I_{FS}$                                     | full scale current                                    |  | 1.95 | 2.30                     | 2.65           | mA              |
| $T_{CFS}$                                    | full scale temperature coefficient                    |  | –    | $\pm 500 \times 10^{-6}$ | –              | $\text{K}^{-1}$ |
| $I_{offset}$                                 | offset current  | $I_{ref} = 0\text{ mA}$                        | –0.1 | 0.0                      | 0.1            | mA              |
| $I_{bias}$                                   | bias current (adjustable)                             |  | –0.6 | –                        | 5.0            | mA              |
| $A_{I_{bias}}$                               | bias current gain                                     |  | 1.9  | 2.0                      | 2.1            |                 |
| <b>Analog outputs (<math>V_{ref}</math>)</b> |   |  |      |                          |                |                 |
| $V_{ref}$                                    | reference voltage output                              |  | 2.10 | 2.20                     | 2.30           | V               |
| $I_{ref}$                                    | reference current output                              |  | –0.3 | –                        | 2.5            | mA              |
| THD  | total harmonic distortion                             | including noise at<br>0 dB;<br>note 3, Fig.7   |      | –75                      | –70            | dB              |
|  |   |  |      | 0.018                    | 0.032          | %               |
| THD  | total harmonic distortion                             | including noise at<br>–60 dB;<br>note 3, Fig.7 | –    | –30                      | –23            | dB              |
|  |   |  | –    | 3.2                      | 7.9            | %               |
| $t_{cs}$                                     | settling time $\pm 1\text{ LSB}$                      |  | –    | 0.5                      | –              | $\mu\text{s}$   |
| $\alpha$                                     | channel separation                                    |  | 85   | 90                       | –              | dB              |
| $ d_{IO} $                                   | unbalance between outputs                             | note 4   | –    | < 0.2                    | 0.3            | dB              |
| $ t_d $                                      | time delay between outputs                            |  | –    | < 0.2                    | –              | $\mu\text{s}$   |
| S/N  | signal-to-noise ratio                                 | at bipolar zero;<br>note 5                     | 90   | 96                       | –              | dB              |

Dual 16-bit DAC (economy version)  
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| SYMBOL                | PARAMETER                   | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-----------------------|-----------------------------|------------|------|------|------|------|
| <b>Timing (Fig.5)</b> |                             |            |      |      |      |      |
| t <sub>r</sub>        | rise time                   |            | –    | –    | 32   | ns   |
| t <sub>f</sub>        | fall time                   |            | –    | –    | 32   | ns   |
| t <sub>CY</sub>       | bit clock cycle time        |            | 108  | –    | –    | ns   |
| t <sub>HB</sub>       | bit clock HIGH time         |            | 22   | –    | –    | ns   |
| t <sub>LB</sub>       | bit clock LOW time          |            | 22   | –    | –    | ns   |
| t <sub>SU;DAT</sub>   | data set-up time            |            | 32   | –    | –    | ns   |
| t <sub>HD;DAT</sub>   | data hold time to bit clock | note 6     | 2    | –    | –    | ns   |
| t <sub>HD;WS</sub>    | word select hold time       | note 6     | 2    | –    | –    | ns   |
| t <sub>SU;WS</sub>    | word select set-up time     |            | 32   | –    | –    | ns   |

**Notes to the characteristics**

1. Measured at I<sub>AOL</sub> = 0 mA and I<sub>AOR</sub> = 0 mA (code 8000H) and I<sub>bias</sub> = 0 mA.
2. V<sub>ripple</sub> = 1% of supply voltage and f<sub>ripple</sub> = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point t<sub>HD;DAT</sub> = 0 ns, this value has been fixed on 2 ns due to tolerances.

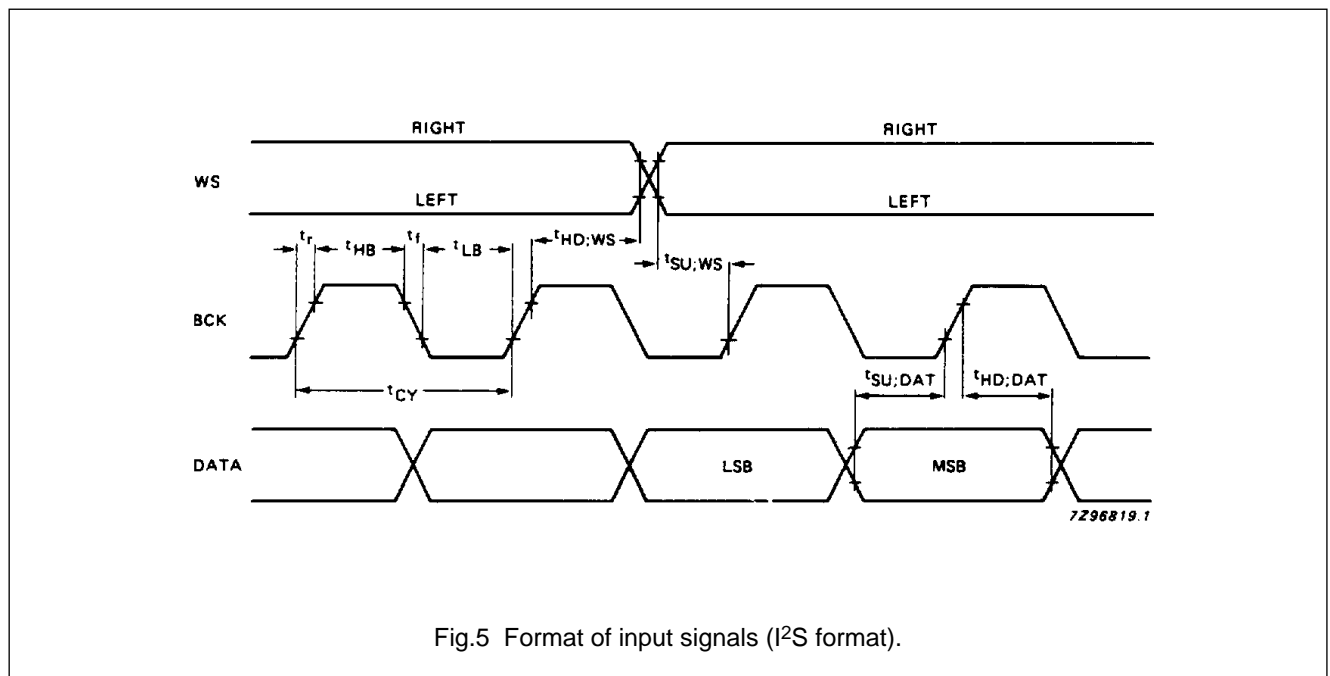


Fig.5 Format of input signals (I<sup>2</sup>S format).



# Dual 16-bit DAC (economy version) (I<sup>2</sup>S input format)

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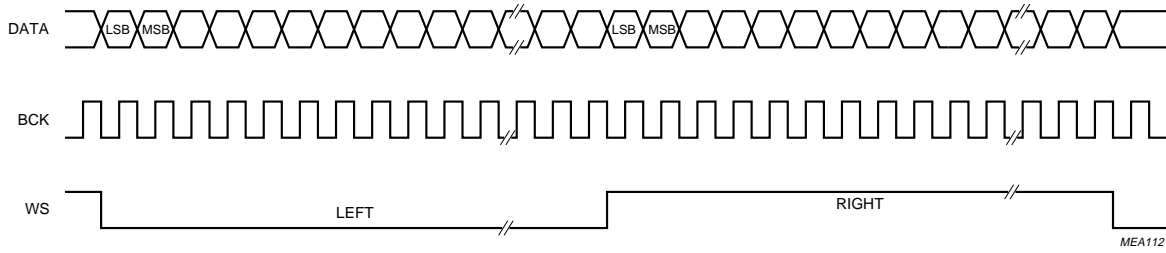
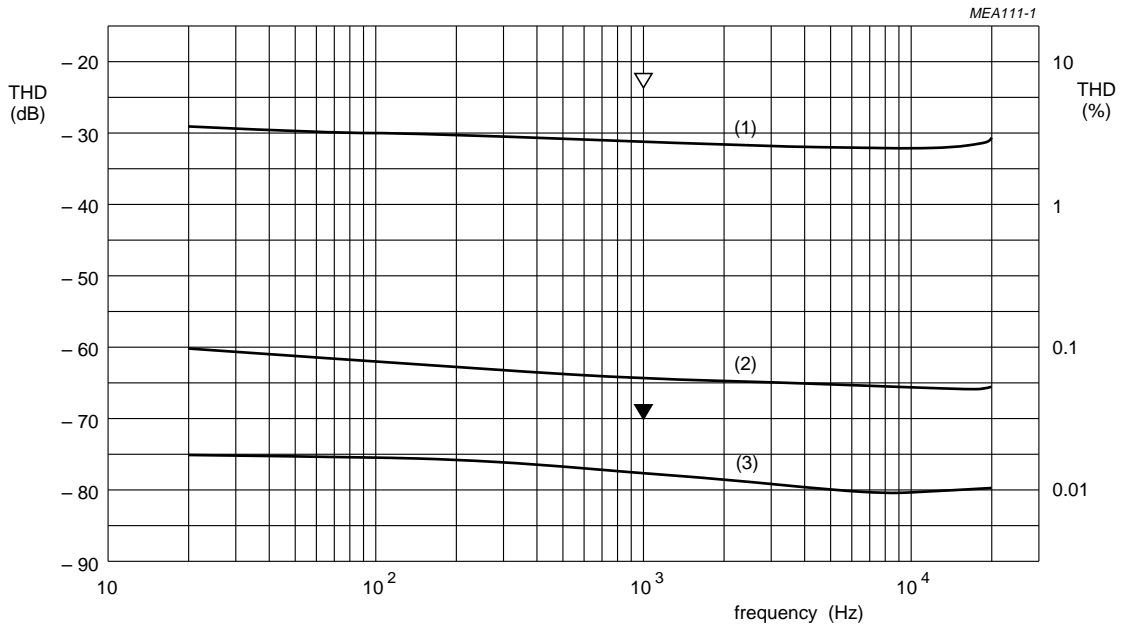


Fig.6 Format of input signals.



- (1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of -60 dB.
- (2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of -24 dB.
- (3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of -0 dB.

Fig.7 Distortion as a function of frequency (4FS).

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**Dual 16-bit DAC (economy version)**  
**(I<sup>2</sup>S input format)**

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**TDA1543****Notes to Fig.7**

- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.
- The arrows indicate the specification limits for 0 dB and –60 dB level signals.

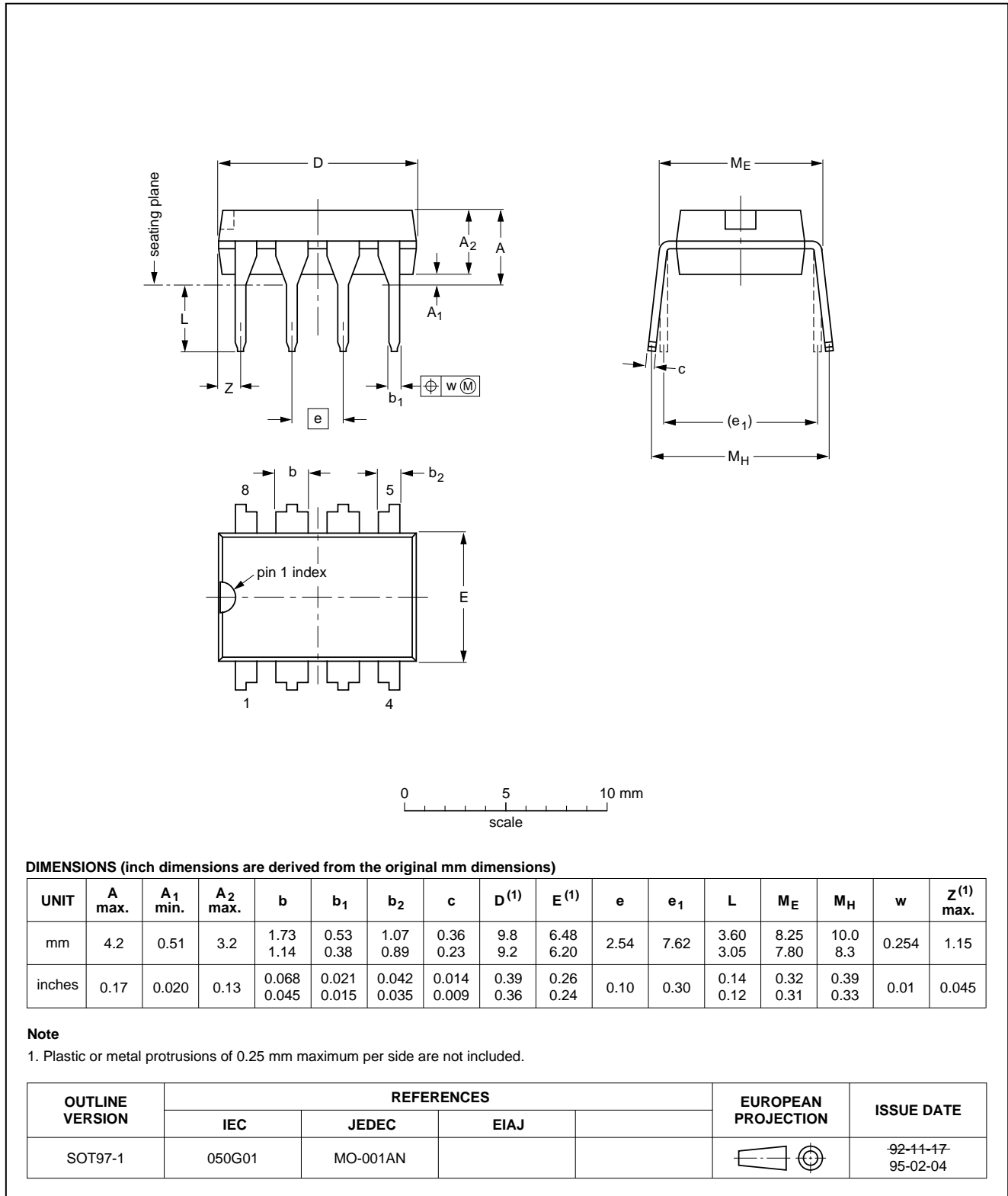
Dual 16-bit DAC (economy version)  
(I<sup>2</sup>S input format)

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PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1

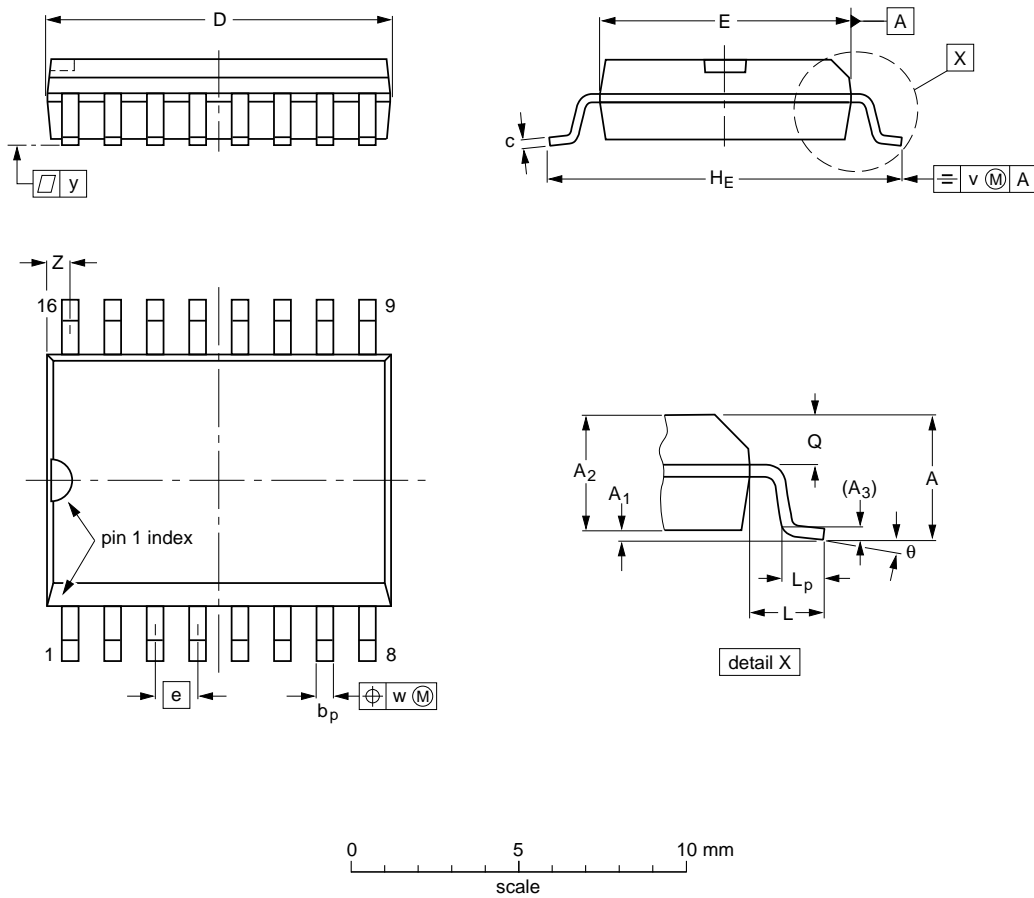


Dual 16-bit DAC (economy version)  
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SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT   | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | Z <sup>(1)</sup> | θ        |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 2.65   | 0.30<br>0.10   | 2.45<br>2.25   | 0.25           | 0.49<br>0.36   | 0.32<br>0.23   | 10.5<br>10.1     | 7.6<br>7.4       | 1.27  | 10.65<br>10.00 | 1.4   | 1.1<br>0.4     | 1.1<br>1.0     | 0.25 | 0.25 | 0.1   | 0.9<br>0.4       | 8°<br>0° |
| inches | 0.10   | 0.012<br>0.004 | 0.096<br>0.089 | 0.01           | 0.019<br>0.014 | 0.013<br>0.009 | 0.41<br>0.40     | 0.30<br>0.29     | 0.050 | 0.42<br>0.39   | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016   |          |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT162-1        | 075E03     | MS-013AA |      |  |                     | 92-11-17<br>95-01-24 |

## Dual 16-bit DAC (economy version) (I<sup>2</sup>S input format)

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### DEFINITIONS

| Data sheet status   |   |
|---|---|
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| Limiting values   |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| Application information   |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

### LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.